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Description

DETECTOR FOR ALPHA PARTICLE OR COSMIC RAY

BACKGROUND OF INVENTION

[0001] The present invention relates generally to a detector circuit and method for sensing an SER (Soft Error Rate) event, such as a strike by an alpha particle or cosmic ray in a silicon substrate, and more particularly pertains to such a detector circuit and method for detecting the floating voltage of a silicon well during a period of non-operation of the circuits fabricated in the silicon well.

SUMMARY OF INVENTION

[0002] Accordingly, it is a primary object of the preset invention to provide a detector circuit and method for sensing an SER event such as an alpha particle or cosmic ray strike in a silicon substrate.

[0003] One significant application for the detection circuit of the present invention is for the redundancy repair latches that are used in SRAMs. The redundancy repair latches are

normally written once at power-up to record failed latch data and are not normally written again. If one of the latches changes states due to an SER (Soft Error Rate-such as a strike by an alpha particle or cosmic ray) event, the repair data in the redundancy latches of the SRAM would now be incorrectly mapped. The detector circuit and method monitors the latches for the occurrence of an SER event, and responsive thereto issues a reload of the repair data to the redundancy repair latches. A first embodiment of the detector circuit differentially detects the floating voltages of first and second silicon wells during periods of non-operation of the circuits fabricated in the first and second silicon wells. In a second embodiment, a detector circuit monitors the background voltage level of a single silicon well over first and second consecutive periods of time.

[0004] A second application for the detection circuit of the present invention is for the detection of an SER event within traditional logic circuits. A traditional clock that controls CMOS circuitry can define when the logic is active (i.e. clock high) versus inactive (i.e. clock low). During the time period when the clock is low, the present invention can be used to detect SER events.

BRIEF DESCRIPTION OF DRAWINGS

[0005] The foregoing objects and advantages of the present invention for a detector circuit and method for sensing an alpha particle or cosmic ray strike circuit may be more readily understood by one skilled in the art with reference being had to the following detailed description of several embodiments thereof, taken in conjunction with the accompanying drawings wherein lime elements are designated by identical reference numerals throughout the several views, and in which:

[0006] Figure 1 illustrates a first embodiment of a detector circuit pursuant to the present invention for detecting an SER event (alpha particle or cosmic ray strike) of a first silicon well or a second silicon well, by differentially detecting the floating voltages of the first and second silicon wells during periods of non-operation of the circuits fabricated in the first and second silicon wells.

[0007] Figure 2 illustrates a second embodiment of the present invention in which a detector circuit monitors a single silicon well in a silicon substrate for an SER event, wherein the silicon well voltage Vwell during a first sampling period of time is compared with the silicon well voltage Vwell over a second sampling period of time to detect a

deviation in the silicon well voltage which is indicative of an SER event.

[0008] Figure 3 illustrates timing diagrams for the clock control signals for the circuit of Figure 2.

DETAILED DESCRIPTION

[0009] After a charged particle, such as an alpha particle or a cosmic ray, passes through silicon, a small but perceptible current flows in the silicon. The present invention provides detector circuits and methods for sensing an alpha particle or cosmic ray strike in a silicon substrate having semiconductor circuits fabricated therein.

[0010] An amplifying detector circuit is connected to the silicon substrate to provide a detectable digital signal when the silicon substrate receives a charged particle strike. A clock signal for clocking and operating the semiconductor circuits fabricated in the silicon substrate serves to specify periods of active and inactive operation of the semiconductor circuits, and the detector is active only when the clock signal is inactive to eliminate false triggering from normal device substrate current flowing during normal switching operations of the semiconductor circuits.

[0011] The present invention provides a detector circuit coupled to a silicon well for detecting a silicon well voltage or cur-

rent to indicate an alpha particle or cosmic ray strike of the silicon well.

[0012] A P well is typically tied high (Vdd) until its off-cycle when it will start drifting down and then if it gets hit by an SER event, the voltage will go slightly lower than a P well that was not hit. An N well is typically tied low (ground) until its off cycle when it will start drifting high and then if it gets hit by an SER event, the voltage in the N well will go slightly higher. The present invention can be used for detecting SER events in both P wells and N wells.

[0013] One significant application for the detection circuit of the present invention is for the redundancy repair latches that are used in SRAMs such as ASIC SRAMs. The redundancy repair latches are normally written once at power-up to record failed latch data and then are never written again. If one of the latches changes states due to an SER (Soft Error Rate-such as a strike by an alpha particle or cosmic ray) event, the repair data in the redundancy latches of the SRAM would now be incorrectly mapped, and thus the SRAM would fail during normal operation. Using the techniques described herein, the present invention monitors the SER activity of the latches and detects the occurrence of an SER event. The system architecture monitors the

output of the SER event detector circuit, and once an SER event is flagged, the system can issue a reload of the repair data to the redundancy repair latches.

[0014] A second application for the detection circuit of the present invention is for the detection of an SER event within traditional logic circuits. A traditional clock that controls CMOS circuitry can define when the logic is active (i.e. clock high) versus inactive (i.e. clock low). During the time period when the clock is low, the present invention can be used to detect SER events.

[0015] Figure 1 illustrates a first embodiment of a detector circuit pursuant to the present invention for detecting an SER event (alpha particle or cosmic ray strike) of a first silicon P well 1 or a second silicon P well 2, by differentially detecting the floating voltages of the first and second silicon wells during periods of non-operation of the circuits fabricated in the first and second silicon wells. Each of the silicon P wells 1 and 2 is connected to two Sense Amps (SA) 1 and 2 which are substantially identical, with Figure 1 only illustrating the circuit details of Sense Amp 1. A single Sense Amp is able to detect that one of the two wells 1 and 2 incurred an SER event, but would not be able to detect which one of the two wells 1 and 2 incurred the

SER event. Two Sense Amps 1 and 2 are provided to be able to detect which one of the two wells 1 and 2 incurred the SER event, as explained below.

[0016] The silicon wells 1 and 2 are connected to their bias power supplies through respective feeder devices 9, 8 which are turned on during normal operation of the circuits defined in the silicon wells 1 and 2. Before a period of normal operation of the circuits, the rising edge of a clk_early signal turns on the Sense Amps 1 and 2 to capture the floating voltages of the wells 1 and 2 in latches defined in the Sense Amps 1 and 2.

[0017] A control logic circuit generates the following control signals:

[0018] 1. Feeder Device Pulse - ON is a pulse which is used to charge the silicon wells 1 and 2 to a full bias potential Vdd by turning on the feeder devices 9, 8. The pulse width of Feeder Device Pulse-On is determined by the time required to charge the silicon wells 1 and 2 to the full bias potential Vdd;

[0019] 2. Feeder Device Pulse - OFF is the period after Feeder Device Pulse - ON, during which the feeder devices 9, 8 are turned off and during which the circuits fabricated in the silicon wells 1 and 2 are inactive, and the voltages of

the silicon wells 1 and 2 are floating;

[0020] 3. A series of clk_early pulses are generated just prior to the start of normal operation of the circuits fabricated in the silicon wells 1 and 2 to drive the detection circuit of Figure 1 to monitor the floating voltages of the silicon wells 1 and 2 for the occurrence of an SER event during the previous inactive floating period. The frequency of the clk_early pulses is determined by the charge rate of the SER event. A simulation has indicated a frequency of about 2ns, which results in a 50mV voltage differential for a 500 um^2 well area.

[0021] The duty cycle of the number of Feeder Device Pulse - ON pulses to the number of clk_early pulses is determined by the leakage rate of the wells. It is important to maximize the time spent sensing versus the time the feeder devices are on.

[0022] To monitor for the occurrence of an SER event, the rising edge of a clk_early pulse on the clock line turns off the devices 7 and 6 to capture the floating voltages of the silicon wells 1 and 2 in latches defined in each of the Sense Amps 1 and 2 at that point in time. Prior thereto, the floating voltages of silicon wells 1 and 2, which had initially been charged to the full bias potential Vdd during

the Feeder Device Pulse - ON, would generally drift downward with time, with the floating voltages of wells 1 and 2 being approximately equal, unless one of the wells incurred an SER event, in which case its floating voltage would be slightly higher. The clk_early pulse turns on the differential sensing and latch circuit within each Sense Amp, which comprises NFET devices 1, 2 and 3 and PFET devices 4 and 5, which amplifies and rectifies any voltage differential between the captured floating voltages of the silicon wells 1 and 2, with the outputs of the two Sense Amps 1 and 2 being input to an XOR gate 11.

[0023] The Sense Amps 1 and 2 can be designed with a built in asymmetry, to establish a preferential set for the latches in SA1 and SA2. The asymmetry can be achieved with offset geometrics between the device sizes in SA1 and SA2. Alternatively a latch could be designed with a preferential set by coupling resistor voltage dividers to each of the two inputs to SA1 and SA2 which would develop unequal voltages at the latch inputs. In this way, the voltages of the two silicon wells 1 and 2, which were initially biased at Vdd, would drop to some voltage over the floating time period, for example to approximately .50Vdd and .55Vdd at the latch inputs.

[0024] The following truth table is for the outputs of SA1 and SA2.

[0025]

Truth Table

SA1	SA2	Result
0	0	OK
0	1	Well #1 error
1	0	Well #2 error
1	1	N/A

[0026] Assume that the Sense Amps have the built in asymmetry described above, such that with no SER event, the sampled floating voltages at the latch inputs would be 0.50Vdd and 0.55Vdd. Sense Amp 1 would produce a 0 output, and Sense Amp 2 would normally produce a 1 output, but the asymmetry would cause Sense Amp 2 to invert its output to produce a 0 output instead. Stated differently, for equal input floating voltages from the wells 1 and 2, the asymmetry results in the 0 0 condition specified in line 1 of the Truth Table, such that the XOR 11 would not produce a 1 detect_error output, the presence of which indicates an SER event. If well 1 incurred an SER event, resulting in a slightly higher floating voltage in well 1 than in well 2, then the Sense Amps 1 and 2 would produce the outputs of line 2 of the Truth Table, resulting in a 1 output from XOR 11, indicating an SER event, with the SA1 output 0

and the SA2 output 1 indicating an SER event in well 1. Similarly, if well 2 incurred an SER event, resulting in a slightly higher floating voltage in well 2 than in well 1, then the Sense Amps 1 and 2 would produce the outputs of line 3 of the Truth Table, resulting in a 1 output from XOR 11, with the SA1 output 1 and the SA2 output 0 indicating an SER event in well 2. The fourth line of the Truth Table is listed but has no realistic meaning whatsoever.

[0027] For the embodiment of Figure 1 for use with an SRAM, the clk_early signal on the clock line would be produced just prior to normal operation of the SRAM, and a 1 output from XOR 11, combined with logic for detecting the conditions of lines 1 and 2 of the Truth Table, would cause the system to issue a reload of the repair data into the redundancy latches of the circuits of well 1 or the circuits of well 2.

[0028] Figure 2 illustrates a second embodiment of the present invention in which a detector circuit monitors a single silicon well in a silicon substrate for an SER event by monitoring the background voltage level of the single silicon well over a period of time. In this embodiment, the silicon well voltage Vwell during a first sampling period of time is compared with the silicon well voltage Vwell over a second

sampling period of time to detect a deviation in the silicon well voltage which is indicative of an SER event. The circuit of Figure 2 is a capacitive sensing detector circuit which takes a correlated double sampling of the background voltage level of the Vwell node voltage to allow offset cancellation of base leakage current and noise current injection of the Vwell node.

[0029] Figure 3 illustrates timing diagrams for the clock control signals for the circuit of Figure 2. In the circuit of Figure 2 the sampled well node voltage Vwell is input to a first device N1 coupled between Vwell and ground and controlled by a first clock signal CK 1. The sampled well node voltage Vwell is also coupled through a second device N2, controlled by a second clock CK2, to the positive input of a differential amplifier. The connection between the second device N2 and the differential amplifier is coupled through a capacitor C1 and a fourth device N4, controlled by the second clock CK2, to ground. A third device N3, controlled by a third clock CK3, is coupled in parallel to the second device N2 and the capacitor C1, between the sampled well node voltage Vwell and the connection between the capacitor C1 and the fourth device N4. A reference circuit is comprised of series connected voltage di-

vider devices N5 and N6, and a voltage divider output therebetween is applied to the negative input of the differential amplifier.

[0030] As illustrated by the circuit of Figure 2 and the timing diagrams of Figure 3, the operation of the circuit is as follows. During a first phase 1, the clocks CK, CK1 and CK2 go high and devices N1, N2 and N4 are turned on, which resets the Vwell node to ground and discharges the capacitor C1 to ground. During a second phase 2, when clock CK1 goes low and clock CK2 remains high, the capacitor C1 charges to the potential of the Vwell node, sensing the background voltage level. During a third phase 3, when clock CK2 goes low and clock CK3 goes high, the voltage across the capacitor C1 is reversed, and the voltage charged during the second clock phase 2 is subtracted from the voltage seen on the Vwell node during the third clock phase (C1=L,C2=L,C3=H).

[0031] If an SER hit is observed in the Vwell node, the injected charge will raise the voltage beyond the background voltage stored on capacitor C1 during the second phase 2, and if it exceeds a threshold voltage provided by the reference circuit of NFET device N5, N6, the comparator will go high to indicate an SER hit.

[0032] While several embodiments and variation of the present invention for a detector circuit and method are described in detail herein, it should be apparent that the disclosure and teachings of the present invention will suggest many alternative designs to those skilled in the art.